What is Claimed Is:

1. A method for designing a semiconductor integrated circuit, comprising the steps of:

providing a cell library that includes gate cell information enabled to execute basic logical functions;

generating a net list by allocating a gate cell stored in said cell library in a logical description described with a register transfer level description; and

verifying whether or not characteristics of said generated net list satisfy a required specification,

wherein said cell library includes information about a plurality of gate cells that execute the same basic logical function but which are characterized by different threshold voltages, and

further wherein each gate cell is allocated in said generating step on a cell allocation condition such that a gate cell with a high threshold voltage of a first insulated gate field effect transistor is selected as a logic gate in which a first insulated gate field effect transistor with a first conductivity is included among a plurality of insulated gate field effect transistors connected serially between operating potential points, while no other insulated gate field effect transistor of the first conductivity type is included along said plurality of insulated gate field effect transistors connected serially between said operating potential points,

and further wherein a gate cell with a low threshold voltage of a second insulated gate field effect transistor is selected as a logic gate in which at least three second insulated gate field effect transistors of the first conductivity type are included among a plurality of said insulated gate field effect transistors connected serially between said operating potential points.

2. The method according to Claim 1, wherein said method further includes another cell allocation condition in which a gate cell with a higher threshold voltage of a third insulated gate field effect transistors is selected from among a plurality of said gate cells included in said cell library as a logic gate in which two third insulated gate field effect transistors of the first conductivity type are included among a plurality of insulated gate field effect transistors connected serially between said operation potential points.

3. The method according to Claim 1, wherein said method further includes another cell allocation condition in which a gate cell with a lower threshold voltage of said first insulated gate field effect transistor is selected from among a plurality of said gate cells included in said cell library as a logic gate in which a first insulated gate field effect transistor is included among a plurality of said insulated gate field effect transistors connected serially between operating potential points, while no insulated gate field effect transistor of the first conductivity type is included among a plurality of said insulated gate field effect transistors connected serially between said operating potential points when said logic gate is required of the ability of driving.

4. The method according to Claim 2, wherein said method further includes another cell allocation condition in which a gate cell with a lower threshold voltage of said first insulated gate field effect transistor is selected from among a plurality of said gate cells included in said cell library as a logic gate in which a first insulated gate field effect transistor is included among a plurality of said insulated gate field effect transistors connected serially between operating potential points, while no insulated gate field effect transistor of the first conductivity type is included among a plurality of said insulated gate field effect transistors connected serially between said operating potential points when said logic gate is required of the ability of driving.

5. The method according to Claim 1, further comprising at least one restriction requirement related to a delay or power consumption requirement of the circuit.

6. A program that includes gate cell information enabled to execute basic logical functions and design a semiconductor integrated circuit by using a cell library that includes information of a plurality of gate cells used to execute the same basic logical function, comprising:

a first subprogram that generates a net list by allocating a gate cell stored in said cell library in a logical description described with a register transfer level description; and

a second subprogram that verifies whether or not characteristics of said generated net list satisfies the required specification;

wherein a gate cell with a higher threshold voltage of a first insulated gate field effect transistor is selected from among a plurality of gate cells included in said cell library as a logic gate in which a first insulated gate field effect transistor of a first conductivity type is included among a plurality of insulated gate field effect transistors connected serially between operating potential points, while a gate cell with a lower threshold voltage of a second insulated gate field effect transistors is selected from among a plurality of said gate cells included in said cell library as a logic gate in which at least three or more second insulated gate field effect transistors of the same conductivity type are included among a plurality of said insulated gate field effect transistors connected serially between said operating potential points upon execution of said first subprogram.

7. The program of Claim 6, wherein the required specification includes at least one restriction requirement related to a delay or power consumption requirement for the circuit.